REMARKS

Claims 21-23, 27-29, 33-35 and 39-41 have been amended to better clarify the invention. No new matter has been entered.

The Examiner's rejection of claims 21, 24, 27, 30, 33, 36, 39, 42, 45, 48, 51 and 54 under 35 USC § 103(a) as being unpatentable over the admitted prior art (APA) in view of Rostoker (U.S. Patent No. 5,399,898), Yoshizaki (U.S. Patent No. 5,475,236) and Liang (U.S. Patent No. 5,952,726) is in error. Amended independent claims 21, 23, 27, 33 and 39 each require that the "two chip electrodes are formed in a common wiring layer of said semiconductor device." The Examiner implicitly admits (Detailed Action, pg. 14), and the Applicant agrees, that APA, Yoshizaki and Liang do not teach this feature.

Yoshizaki discloses such a configuration wherein a solder bump 22 is connected to an electrode pattern 204 via a contact hole 205a that is filled by a conductor. The electrode pattern 204 is connected to each of two different interconnection electrodes 201c via the respective contact holes 203a that are filled with the electrode pattern 204 (Fig. 7).

In other words, Yoshizaki discloses a configuration in which two different interconnection electrodes 201c are connected to the solder bump 22, not directly, but via the electrode pattern 204, and the contact holes 203a and 205a. Alternatively, in the claimed invention, the bumps are connected to a common wiring layer of a semiconductor chip via chip electrodes. Thus, Yoshizaki cannot render obvious this aspect of claims 21, 24, 27, 30, 33, 36, 39, 42, 45, 48, 51 and 54.

The Examiner takes the position that the missing feature of Yoshizaki and Liang is found in Rostoker. According to the Examiner, "[R]ostoker shows the electrode set comprising two

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electrodes (222 c and d) being connected to a common internal conductor/wiring layer of the chip (235a/224 in Fig 2b; col. 11, line 23 - col. 12, line 13)." Applicant submits that Fig. 2b cannot teach "at least two electrodes" because Fig. 2b does not contain any electrodes! Elements 222c and 222d, which the Examiner labels as electrodes, are not electrodes but external bump pads (col. 11, line 60; col. 12, line 9).

Further, Rostoker discloses jumpering bump contacts, or bump contacts 222c and 222d, that are respectively connected to an internal conductor 236b via either one of conductive plugs 234a and 234b (col. 11, lines 59-60 and Fig. 2b). As shown in Figs. 5a and 5b, when a flip-chip, or a semiconductor chip with bumps, is mounted on a wiring substrate, jumpered contacts are used to solve routing problems in a flip-chip assembly by providing an effective "extra" layer of wiring, thus helping to keep signal paths on the wiring substrate in such assemblies as short and as simple possible (col. 12, lines 14-17).

Thus, the bump contacts 222c and 222d are not used in such a manner that would enable them to be connected to the same wiring on the wiring substrate. Therefore, Rostoker neither discloses nor suggests the claimed invention's feature that at least two chip electrodes are connected to a same wiring of the wiring substrate via bumps. And, Rostoker does not teach the feature the Examiner acknowledges is missing from the other reference, no combination of APA, Yoshizaki, Rostoker and Liang could achieve or render obvious Applicant's invention.

Claims 22, 25, 28, 31, 34, 37, 40, 43, 46, 49, 52 and 55 similarly are improperly rejected under 35 USC § 103(a) as being unpatentable over the APA in view of Yoshizaki, Rostoker, Liang and Fulcher (U.S. Patent No. 5,686,764). Independent claims 22, 28, 34 and 40 contain the same features as discussed above. APA, Yoshizaki, Rostoker and Liang do not teach two

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chip electrodes formed in a common wiring layer. Fulcher also fails to provide the above discussed missing teaching. Therefore, this combination of art also does not achieve or render obvious Applicant's invention.

Finally, the Examiner improperly rejected claims 23, 26 ,29 ,32, 35, 38, 41, 44, 47, 50, 53 and 56 under 35 USC § 103(a) as being unpatentable over the APA in view of Yoshizaki, Rostoker, Liang and Bertolet et al. (U.S. Patent No. 5,844,317). Bertolet et al. also does not provide the above discussed missing teaching. Bertolet et al. teaches a wire bonding pad of the die beneath the conductive strap. Thus, because these claims contain the same limitations discussed *supra*, they are likewise patentable.

The foregoing Amendment raises no new issues which require further search or consideration by the Examiner. Accordingly, entry of the foregoing Amendment and allowance of the Application are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,

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I hereby certify that this correspondence is being sent via facsimile to EXAMINER NITIN PAREKH of the United States Patent and Trademark Office at facsimile number (703) 872-9319, on August 20, 2003 from Tucson, Arizona.

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